Docket No.: 10017911-1-3-Streeter (1509-240A) PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

KOCH II, KENNETH

U.S. Patent Application No. 10/777,174 : Group Art Unit: 2816

Filed: February 13, 2004 : Examiner: LONG T NGUYEN

For: DRIVER CIRCUIT CONNECTED TO PULSE SHAPING CIRCUITRY

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Declaration of Kenneth Koch II

I, Kenneth Koch, II, hereby declare as follows:

1. I and others consider that I am an expert in the design and operation of electronic circuits. In fact, my current job title with my current employer, Hewlett Packard, Co., (HP), is "Expert." One particular area of expertise I have concerns the design and analysis of electronic circuits including field effect transistors that function as voltage controlled capacitors that switch from a finite capacitance value to a substantially open circuit in response to the voltage across the capacitor changing between opposite sides of a voltage threshold.

2. The opinions expressed in paragraph 1 are based on my background which is as follows:

Education: In 1981, I was awarded a Bachelor of Science Degree in Electrical Engineering from Southern Massachusetts University.

Work experience: Between 1981 and 1990, I worked as an electronic engineer, designing communications hardware at American Telephone and Telegraphic Co., Fibronics, Telco Systems, and Apollo Computer. Between 1990 and 1999 I was a designer of very large scale integrated

(VLSI) circuits at Hewlett Packard, designing full custom circuits and logic blocks, developed design tools and designed analog and digital circuits. Between 1999 and 2005, while employed by Hewlett Packard, I have designed methods for enabling other engineers to design VLSI circuits. My current job includes defining the scope and schedule for various projects, as well as some design work. A notable skill I have is the ability to design techniques to reduce the effort and time required to complete a project.

I led a team of 3 engineers to successfully design the input-output circuits for a commercially successful 4 Gigabyte per second memory bus. This circuitry is 25% "faster" than the design of a leading integrated circuit manufacturer. This design also included "hooks" for enabling the number of CPUs connected to this bus to be doubled.

I designed methods used by about 100 designers to leverage a single CPU manufactured in a .13um process into a dual 1GHz CPU chip manufactured with a .1um process. This included leading a team of 6 engineers and using data driven arguments to reduce scope by about 32 MYs.

I designed methods of porting a CPU from a standard bulk CMOS process into a CMOS circuit using capacitors that are switched in response to the voltage across the capacitors crossing a threshold. This included creating new circuits now patented, as U.S. Patents 6,759,880 and 6,753,708.

I am patentee of at least six other issued U.S. patents: 6,882,201; 6,803,783; 6,778,111; 6,734,709; 6,404,243 and 5,692,026.

I defined and tested Hewlett-Packard's Electrical Rules Check software. This included defining the software used by Hewlett-Packard to check for cross talk problems.

I designed hand held equipment used to test IBM system 36 and 3270 networks.

I designed a CEPT/T1 interface to a microwave radio. This included a transmitter, receiver, phase lock loops, synchronization and FPGA design.

I designed a 560Mb/s laser driver (1986) and laser temperature controller for an FO repeater.

I was a member of ANSI's FDDI low cost fiber optic standards committee.

Every design that I ever worked on has been successful. This includes over 15 projects.

I am also skilled in the following areas:

VLSI, analog, digital, PCB, FPGA, phase located loops, PLL, Control loop, Fiber Optic, design experiences, kshell and perl scripting, SPICE, transmission lines, synthesis CELL3, CAD tools including Mentor, Cadence, Orcad, Viewlogic, test vector generation with sunrise, verilog, veritime and HP's Chip Buster.

3. I have thoroughly considered Hamasaki et al., U.S. Patent 5,694,065. It is my understanding that the Examiner has stated that it would have been obvious to one or ordinary skill in the art to have replaced the capacitors illustrated in Figures 4 and 5 of Hamasaki et al., that are employed as capacitors C_n and C_p in the circuit of Figure 2, with field effect transistors such that capacitor C_n is replaced by an n-channel field effect transistor. The circuit of my application includes a showing of an n-channel field effect transistor, (that functions as a capacitor) connected between the gate of a p-channel transistor and ground and a p-channel field effect transistor (that functions as a capacitor) connected between the gate of an n-channel transistor and a positive power supply terminal. Hence, the only logical substitution to meet the Examiner's concern relates to replacing capacitor C_n with an n-channel field effect transistor that functions as a capacitor. Replacing capacitor C_p with a p-channel field effect transistor that functions as a capacitor is not appropriate because the p-channel field effect transistor of my circuit is connected between the gate of the n-channel transistor and the positive power supply terminal. In the Hamasaki et al. circuit, one electrode of the capacitor is connected to the gate of the n-channel field effect transistor and the other electrode is grounded.

4. I do not believe one of ordinary skill in the art would have replaced capacitor C_n, as illustrated in Figures 4 and 5 of Hamasaki et al. with an n-channel field effect transistor connected as a capacitor. I do not agree with the Examiner's statement that such a substitution would have been made by one of ordinary skill in the art because of greater efficiency. In fact, if possible, designers of electronic circuits generally avoid the use of field effect transistor devices that are connected in the capacitance mode. This is because field effect transistors connected in the capacitance mode have significant channel and diffusion resistance. The channel and diffusion resistance is usually in the thousands of ohms/square range, which results in the field effect transistor not behaving like a capacitor at higher frequencies. The value of the channel and diffusion resistance is usually poorly controlled by manufacturers of integrated circuits. A further disadvantage of using field effect transistor devices as capacitors is that the field effect transistor gate to channel capacity is a function of the gate to channel voltage, resulting in a capacitor with a capacitance that may be difficult to control. To obtain the maximum capacitance per unit area, the field effect transistor must be biased to an on state. A further disadvantage in using field effect transistors as capacitors is the gate leakage current. When the field effect transistor is biased in the linear or saturation region the gate leakage current, i.e., the current that leaks from the gate to the channel, can be large enough to affect the performance of the circuit in an adverse manner. The gate leakage current also is a concern because many manufacturers do not provide a field effect transistor model which accurately indicates gate leakage current, if they indicate it at all. Without an accurate indication of gate leakage current, the designer is likely to make poor choices. In addition, a discrete capacitor, such as the capacitor disclosed in Figures 4 and 5 of the Hamasaki et al. reference functions as a capacitor to a much greater extent than a field effect transistor that is connected in a capacitor mode.

5. We decided to use an n-channel field effect transistor (that functions as a capacitor) with a connection between the gate of a p-channel transistor and ground, i.e., in shunt between the gate of the p-channel transistor and ground, because of the capability of such a transistor achieving desirable switching effects. These switching effects are achieved in a very simple manner by using such an n-channel field effect transistor, connected in a capacitance mode.

6. Based on the foregoing, in my opinion, one of ordinary skill in the art would not, upon studying and/or using the Hamasaki et al. circuit of Figure 2 have replaced capacitor C_n as illustrated in Figures 4 and 5, with an n-channel field effect transistor, connected in a capacitance mode.

7. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated this 17 day of May, 2005 at Ft Collins, Colorado.

Kenneth Koch, II

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CERTIFICATION OF FACSIMILE TRANSMISSION
I HEREBY CERTIFY THAT THIS PAPER IS BEING FACSIMILE TRANSMITTED TO THE PATENT AND TRADEMARK OFFICE ON THE DATE SHOWN BELOW

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